



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,007	07/30/2003	Yi Ding	M-15223 US	2298

7590 03/26/2004

Michael Shenker  
MacPHERSON KWOK CHEN & HEID LLP  
Suite 226  
1762 Technology Drive  
San Jose, CA 95110

EXAMINER

SOWARD, IDA M

ART UNIT PAPER NUMBER

2822

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/632,007

Applicant(s)

DING, YI

Examiner

Ida M Soward

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>7-30-03 &amp; 9-22-03</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

This Office Action is in response to the application filed July 30, 2003.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 1-8 in view of Wang (US 2004/0004863 A1).

In regard to claim 1, Admitted Prior Art Figures 1-8 teach an array of nonvolatile memory cells, each cell comprising a first conductive gate 140, two conductive floating gates 160, and two source/drain regions 174, the source/drain regions being regions of a first conductivity type in a semiconductor substrate.

However, Admitted Prior Art Figures 1-8 fail to teach in each row of the array, all the first conductive gates are connected together; wherein in each column of the array, for any two consecutive memory cells, one source/drain region of one of the cells and one source/drain region of the other one of the cells are provided by a contiguous region of the first conductivity type in the semiconductor substrate, each contiguous region providing source/drain regions to only two of the memory cells in said column of the memory cells; wherein the array also comprises a plurality of bitlines overlying the

semiconductor substrate, the bitlines being connected to the source/drain regions of the memory cells.

In regard to claim 1, Wang teaches teach in each row of the array, all the first conductive gates 100 are connected together; wherein in each column of the array, for any two consecutive memory cells, one source/drain region 22/24 of one of the cells and one source/drain region of the other one of the cells are provided by a contiguous region of the first conductivity type in the semiconductor substrate, each contiguous region providing source/drain regions to only two of the memory cells in said column of the memory cells; wherein the array also comprises a plurality of bitlines 23 overlying the semiconductor substrate, the bitlines being connected to the source/drain regions of the memory cells (Figures 30-31, pages 16-17, paragraphs [0115]-[0118], respectively).

In regard to claim 2, Wang teaches at least one bitline is connected to one source/drain region of each memory cell in two columns of the memory cells (Figure 31).

In regard to claim 3, Wang teaches in said two columns of the memory cells, the source/drain regions of one of the columns are separated from the source/drain regions of the other one of the columns by field isolation regions 5 in the semiconductor substrate (Figures 4-4A, page 6, paragraph [0059]).

In regard to claim 4, Wang teaches at least two columns of the memory cells, at least one contiguous region provides exactly two source/drain 22/24 regions for one of the columns and exactly two source/drain 22-24 regions in the other one of the columns (Figure 31).

In regard to claim 5, Wang teaches each memory cell has one of its source/drain regions 22/24 connected to one of the bitlines 23, and the other one of its source/drain regions 22/24 connected to another one of the bitlines 23 (Figure 31).

In regard to claim 6, Wang teaches each memory cell also comprises two second conductive gates 15 & 20, and in each row one second conductive gate of each memory cell is connected to one second conductive gate of every other memory cell in that row (Figures 30-31, pages 16-17, paragraphs [0115]-[0118], respectively).

In regard to claim 7, Wang teaches the first conductive gates 10 in each row are provided by a first conductive line 15a formed over the semiconductor substrate; and for each row, the array has two second conductive lines over the semiconductor substrate, each of the second conductive lines providing one second conductive gate to each memory cell in the row (Figures 30-31, pages 16-17, paragraphs [0115]-[0118], respectively).

Since the method claims 8-14 only recites all the limitations of the array of nonvolatile memory cells in claims 1-7, Admitted Prior Art Figures 1-8 and Wang also disclose all the limitations in method claims 8-14 as well.

Since Admitted Prior Art Figures 1-8 and Wang are from the same field of endeavor (nonvolatile memory cells), the purpose disclosed by Wang would have been pertinent in the art of Admitted Prior Art Figures 1-8. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the nonvolatile memory cell structure as taught by Admitted Prior Art Figures 1-8 with the nonvolatile memory cell structure having columns of memory cells as taught by

Wang to provide the capability of arranging the memory array in other configurations or a combination thereof (page 17, paragraph [0119]).

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to nonvolatile memory cell arrays:

Kobatake (EP 0938098 A2)

Park et al. (US 2003/0218908 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2822

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS

March 18, 2004

  
AMIR ZARABIAN  
LEAD PATENT EXAMINER  
MARCH 2004